

REMARKS

Claims 1, 6, 7, 9-13, 15, 17, 18, 20-23, 25-27, 44, 52, 58, and 61-77 are pending. Claims 1, 7, 11, 12, 15, 17, 20-22, 25-27, 44, 61, 62, 66, 68-71, and 73-77 have been amended.

The amendment filed April 28, 2003 has been objected to under 35 U.S.C. § 132 as introducing new matter, and claims 7, 9, and 13 stand rejected under 35 U.S.C. § 112, first paragraph as containing subject matter not described in the specification. Claim 7 has been amended to address the Examiner's concerns, and is submitted along with its dependent claims 9 and 13 as being fully supported by the specification. Withdrawal of this rejection is requested.

Claims 1, 6, 7, 9, 17, 18, 20, 24, 26, 44, 61, 68, 75, 76, and 77 stand rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Pat. No. 5,275,184 to Nishizawa et al. Applicant traverses this rejection.

Claim 1 recites a method for "removing surface contaminants from an air/liquid interface of a semiconductor processing bath for processing semiconductor wafers." The method includes "immersing wafers in a bath of semiconductor processing fluid," "processing said wafers immersed in said bath of semiconductor processing fluid contained within said processing apparatus," and "reducing an overall volume capacity of said processing apparatus, thereby rapidly displacing an upper portion of said semiconductor processing fluid from said processing apparatus while said wafers remain fully immersed in a lower portion of said semiconductor processing fluid within said processing apparatus to remove said surface contaminants from said air/liquid interface."

Nishizawa discloses a wafer treatment method using a continuous flow of fluids maintained at a constant volume. Nishizawa does not teach or suggest a method for

“removing surface contaminants from an air/liquid interface of a semiconductor processing bath for processing semiconductor wafers” which includes “reducing an overall volume capacity of said processing apparatus, thereby rapidly displacing an upper portion of said semiconductor processing fluid from said processing apparatus while said wafers remain fully immersed in a lower portion of said semiconductor processing fluid within said processing apparatus to remove said surface contaminants from said air/liquid interface.” Nishizawa does not anticipate or render obvious claim 1 or its dependent claim 6.

Claim 7 recites a method for “reducing the contamination on a semiconductor wafer from a wet etching bath.” The method includes “immersing said semiconductor wafer in said wet etching bath,” “processing said semiconductor wafer in said wet etching bath by continuously feeding an etching fluid,” “stopping the continuous feeding of etching fluid,” “subsequently rapidly reducing a volume of said wet etching bath contained within a processing apparatus by removing an upper portion of said etching fluid from said processing apparatus to reduce an overall volume of etching fluid in said processing apparatus and remove surface contaminants from an air/liquid interface of said wet etching bath while retaining said semiconductor wafer fully immersed in a lower portion of said etching fluid contained within said processing apparatus,” and “subsequently removing said semiconductor wafer from said wet etching bath.”

Nishizawa et al. discloses a wafer treatment method with a continuous flow of etching fluid at a constant volume. Nishizawa et al. does not teach or suggest a method for “reducing the contamination on a semiconductor wafer from a wet etching bath” which includes “stopping the continuous feeding of etching fluid,” “subsequently rapidly reducing a volume of said wet etching bath contained within a processing apparatus by removing an upper portion of said etching fluid from said processing apparatus to reduce an overall volume of etching fluid in said processing apparatus and remove surface contaminants from an air/liquid interface of said wet etching bath while retaining said

semiconductor wafer fully immersed in a lower portion of said etching fluid contained within said processing apparatus,” and “subsequently removing said semiconductor wafer from said wet etching bath.” Claim 7, and its dependent claims 9, 10, and 13, are not anticipated or rendered obvious by Nishizawa et al.

Claim 17 recites a method for etching a semiconductor wafer.” The method includes “placing an aqueous hydrofluoric acid etching fluid into a wet etching vessel,” “immersing said semiconductor wafer in a process volume of said etching fluid,” “contacting said semiconductor wafer with said etching fluid for a predetermined time,” “reducing a volume of said etching fluid contained in said wet etching vessel by rapidly removing an upper portion of said etching fluid from the top of said wet etching vessel while keeping said semiconductor wafer immersed to obtain a remaining portion of said etching fluid, said remaining portion having a smaller volume than said process volume,” and “removing said semiconductor wafer from said remaining portion of said etching fluid.”

Nishizawa et al. teaches a dipping type wafer treatment method with a continuous flow of fluids at a constant volume. Nishizawa et al. does not teach or suggest a method for etching a semiconductor wafer which includes “reducing a volume of said etching fluid contained in said wet etching vessel by rapidly removing an upper portion of said etching fluid from the top of said wet etching vessel while keeping said semiconductor wafer immersed to obtain a remaining portion of said etching fluid, said remaining portion having a smaller volume than said process volume,” and “removing said semiconductor wafer from said remaining portion of said etching fluid.” Claim 17, and its dependent claims 18, 20, and 26, are not anticipated or rendered obvious by Nishizawa et al.

Claim 44 recites a “method for reducing the contaminants on a silicon wafer during a wet etching process.” The method includes “immersing a wafer boat suspended

on a lifting arm in an etching vessel having an aqueous hydrofluoric acid solution therein for a sufficient time to etch said silicon wafer,” “continuously feeding said aqueous hydrofluoric acid solution to process said semiconductor wafer,” “stopping said continuous feeding of acid solution,” and “rapidly removing said wafer boat from said etching vessel to remove surface contaminants residing on the upper surface of said aqueous hydrofluoric acid solution by an upward movement of said arm, thereby causing an upper portion of said aqueous hydrofluoric acid solution to spill out of said vessel to reduce the amount of said aqueous hydrofluoric acid solution in said etching vessel.”

Nishizawa et al. discloses a wafer treatment method having a continuous flow of treatment fluids. Nishizawa et al. does not teach or suggest “method for reducing the contaminants on a silicon wafer during a wet etching process” as recited in claim 44. Whereas Nishizawa et al. includes continuously feeding an acid etching solution to process a semiconductor wafer, Nishizawa et al. does not disclose “stopping said continuous feeding of acid solution,” and “rapidly removing said wafer boat from said etching vessel to remove surface contaminants residing on the upper surface of said aqueous hydrofluoric acid solution by an upward movement of said arm, thereby causing an upper portion of said aqueous hydrofluoric acid solution to spill out of said vessel to reduce the amount of said aqueous hydrofluoric acid solution in said etching vessel.” Claim 44 is not anticipated or rendered obvious by Nishizawa et al.

Claim 61 recites “a method for removing surface contaminants from an air/liquid interface of a semiconductor processing bath for processing semiconductor wafers.” The method includes “immersing said semiconductor wafers in said semiconductor processing bath contained in a processing apparatus,” and “reducing a volume of said semiconductor processing bath contained within said processing apparatus by rapidly removing an upper portion of said semiconductor processing fluid present in said processing apparatus, while said wafers are immersed in a remaining lower portion of

said bath, to permit flow of said upper portion of said processing fluid out of said processing apparatus and reduce a total volume of fluid contained within said processing apparatus and thereby break eddy currents holding said surface contaminants at said air/liquid interface.”

Nishizawa et al. discloses a wafer treatment method in which contaminants are avoided by a continuous flow of a constant volume of treatment fluids. Nishizawa et al. does not teach or suggest “a method for removing surface contaminants from an air/liquid interface of a semiconductor processing bath for processing semiconductor wafers” which includes “reducing a volume of said semiconductor processing bath contained within said processing apparatus by rapidly removing an upper portion of said semiconductor processing fluid present in said processing apparatus, while said wafers are immersed in a remaining lower portion of said bath, to permit flow of said upper portion of said processing fluid out of said processing apparatus and reduce a total volume of fluid contained within said processing apparatus and thereby break eddy currents holding said surface contaminants at said air/liquid interface.” Claim 61, and its dependent claims 62, 63, 64, and 67 are not anticipated or rendered obvious by Nishizawa et al.

Claim 68 recites “a method for removing surface contaminants from an air/liquid interface of a semiconductor processing bath for processing semiconductor wafers.” The method includes “processing said semiconductor wafers in a semiconductor processing bath having a volume,” “reducing said volume of said semiconductor processing bath in a processing vessel by rapidly removing an upper portion of a semiconductor processing fluid present in said processing vessel, while said wafers are immersed in a remaining lower portion of said semiconductor processing fluid in said bath, to permit flow of said upper portion of said processing fluid and thereby break surface tension forces holding said surface contaminants at said air/liquid interface, an overall volume of fluid remaining in said processing vessel being less than said processing bath volume,” and

“removing said semiconductor_wafers from said remaining lower portion of said semiconductor processing fluid.”

Nishizawa et al. discloses a wafer treatment method which uses a continuous flow of a constant volume of treatment fluids. Nishizawa et al. does not teach or suggest “a method for removing surface contaminants from an air/liquid interface of a semiconductor processing bath for processing semiconductor wafers” which includes “processing said semiconductor wafers in a semiconductor processing bath having a volume,” “reducing said volume of said semiconductor processing bath in a processing vessel by rapidly removing an upper portion of a semiconductor processing fluid present in said processing vessel, while said wafers are immersed in a remaining lower portion of said semiconductor processing fluid in said bath, to permit flow of said upper portion of said processing fluid and thereby break surface tension forces holding said surface contaminants at said air/liquid interface, an overall volume of fluid remaining in said processing vessel being less than said volume,” and “removing said semiconductor_wafers from said remaining lower portion of said semiconductor processing fluid.” Nishizawa et al. does not anticipate or render obvious claim 68, or its dependent claims 69-71 and 74.

Claim 75 recites “a method for reducing the contamination on a semiconductor wafer from a wet etching bath.” The method includes “processing said semiconductor wafer in said wet etching bath containing an etching fluid,” “subsequently reducing a volume of etching fluid in said wet etching bath and breaking eddy currents of said wet etching bath by rapidly removing an upper portion of said etching fluid from a processing vessel containing said wet etching bath to reduce an overall volume of fluid contained within said processing vessel, said act of breaking said eddy currents further releasing surface contaminants which are formed at an air/liquid interface of said wet etching bath and held at said air/liquid interface by said eddy currents,” and “subsequently removing said semiconductor wafer from said reduced overall volume of said wet etching bath.”

The wafer treatment method of Nishizawa et al. does not include “reducing a volume of etching fluid in said wet etching bath and breaking eddy currents of said wet etching bath by rapidly removing an upper portion of said etching fluid from a processing vessel containing said wet etching bath to reduce an overall volume of fluid contained within said processing vessel, said act of breaking said eddy currents further releasing surface contaminants which are formed at an air/liquid interface of said wet etching bath and held at said air/liquid interface by said eddy currents,” and “subsequently removing said semiconductor wafer from said reduced overall volume of said wet etching bath.” Claim 75 is not anticipated or rendered obvious by Nishizawa et al.

Claim 76 recites “a method for reducing the contamination on a semiconductor wafer from a wet etching bath.” The method includes “processing said semiconductor wafer in said wet etching bath containing an etching fluid completely filling a processing vessel,” “subsequently reducing a volume of said wet etching fluid and breaking surface tension forces of said wet etching bath by rapidly removing an upper portion of said etching fluid from said processing vessel containing said wet etching bath and reduce an overall volume of fluid contained within said processing vessel such that said processing vessel is no longer full, said act of breaking said surface tension forces further releasing surface contaminants which are formed at an air/liquid interface of said wet etching bath and held at said air/liquid interface by said eddy currents,” and “subsequently removing said semiconductor wafer from said wet etching bath having a reduced overall volume of fluid.”

The method of Nishizawa et al. uses a continuous flow of treatment fluids at a constant volume. Nishizawa et al. does not teach or suggest “a method for reducing the contamination on a semiconductor wafer from a wet etching bath” which includes “reducing a volume of said wet etching fluid and breaking surface tension forces of said wet etching bath by rapidly removing an upper portion of said etching fluid from said

processing vessel containing said wet etching bath and reduce an overall volume of fluid contained within said processing vessel such that said processing vessel is no longer full, said act of breaking said surface tension forces further releasing surface contaminants which are formed at an air/liquid interface of said wet etching bath and held at said air/liquid interface by said eddy currents,” and “subsequently removing said semiconductor wafer from said wet etching bath having a reduced overall volume of fluid.” Claim 76 is not anticipated or rendered obvious by Nishizawa et al.

Claim 77 recites “a method for reducing the contamination on a semiconductor wafer.” The method includes “processing said semiconductor wafer immersed in a static etching bath containing an etching fluid,” and “reducing a volume of said etching fluid by rapidly removing an upper portion of said etching fluid from a container holding said static etching bath to reduce an overall volume of fluid contained within said container, such that said container holds less fluid while said semiconductor wafer is immersed in a remaining portion of said static etching bath.”

Nishizawa et al. discloses a wafer treatment method which uses a continuous flow of fluids. Nishizawa et al. does not teach or suggest “a method for reducing the contamination on a semiconductor wafer” which includes “processing said semiconductor wafer immersed in a static etching bath containing an etching fluid,” and “reducing a volume of said etching fluid by rapidly removing an upper portion of said etching fluid from a container holding said static etching bath to reduce an overall volume of fluid contained within said container, such that said container holds less fluid while said semiconductor wafer is immersed in a remaining portion of said static etching bath.” Nishizawa et al. does not anticipate or render obvious claim 77.

Claims 11 and 21 stand rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Pat. No. 5,656,097 to Olesen et al. Applicant traverses this rejection.

Claim 11 recites “a method for removing surface contaminants from an air/liquid interface of a semiconductor processing bath for processing semiconductor wafers.” The method includes “immersing wafers in said semiconductor processing bath,” “reducing a volume of said semiconductor processing bath contained within a processing apparatus by rapidly removing from a top of said processing apparatus an upper surface portion of a semiconductor processing fluid present in said bath to rapidly reduce said volume of said processing bath contained within said processing apparatus, while said wafers are immersed in said bath, by opening a valve in said processing apparatus to remove said surface contaminants from said air/liquid interface,” and “removing said wafers from said semiconductor processing bath.”

Olesen et al. discloses a wafer cleaning tank with a pneumatic “quick dump” valve disposed on the tank bottom. Olesen et al. does not teach or suggest “a method for removing surface contaminants from an air/liquid interface of a semiconductor processing bath for processing semiconductor wafers” that includes “reducing a volume of said semiconductor processing bath contained within a processing apparatus by rapidly removing from a top of said processing apparatus an upper surface portion of a semiconductor processing fluid present in said bath to rapidly reduce said volume of said processing bath contained within said processing apparatus, while said wafers are immersed in said bath, by opening a valve in said processing apparatus to remove said surface contaminants from said air/liquid interface,” and “removing said wafers from said semiconductor processing bath.” Olesen et al. does not anticipate or render obvious claim 11.

Claim 21 recites “a method for etching a semiconductor wafer” that includes “placing an etching fluid into a wet etching vessel,” “placing said semiconductor wafer in said etching fluid,” “contacting said semiconductor wafer with said etching fluid for a predetermined time,” and “reducing a volume capacity of said wet etching vessel, thereby rapidly removing a portion of said etching fluid from the top of said wet etching vessel by opening a valve to reduce rapidly an overall volume of fluid in said wet etching vessel while said semiconductor wafer remains immersed in a lower portion of said etching fluid.”

Olesen et al. discloses cleaning tank with a quick dump valve located in the bottom of the tank. Olesen et al. does not disclose or suggest “a method for etching a semiconductor wafer” that includes “reducing a volume capacity of said wet etching vessel, thereby rapidly removing a portion of said etching fluid from the top of said wet etching vessel by opening a valve to reduce rapidly an overall volume of fluid in said wet etching vessel while said semiconductor wafer remains immersed in a lower portion of said etching fluid.” Olesen et al. does not anticipate or render obvious claim 21.

Claims 66 and 73 stand rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Pat. No. 6,131,588 to Kamikawa et al. Applicant traverses this rejection.

Claim 66 recites “a method for removing surface contaminants from an air/liquid interface of a semiconductor processing bath for processing semiconductor wafers.” The method includes “immersing said semiconductor wafers in a semiconductor etching bath,” and “rapidly removing an upper portion of a semiconductor processing fluid present in said etching bath by rapidly removing a wafer boat containing said wafers from said bath, to permit flow of said upper portion of said processing fluid and thereby break eddy currents holding said surface contaminants at said air/liquid interface.”

Kamikawa et al. discloses a wafer cleaning method in which a wafer cleaning solution is replaced by deionized water before the wafers are removed from the cleaning bath and moved up to a drying chamber. Kamikawa et al. does not disclose or suggest “a method for removing surface contaminants from an air/liquid interface of a semiconductor processing bath for processing semiconductor wafers” that includes “immersing said semiconductor wafers in a semiconductor etching bath,” and “rapidly removing an upper portion of a semiconductor processing fluid present in said etching bath by rapidly removing a wafer boat containing said wafers from said bath, to permit flow of said upper portion of said processing fluid and thereby break eddy currents holding said surface contaminants at said air/liquid interface.” Kamikawa et al. does not anticipate or render obvious claim 66.

Claim 73 recites “a method for removing surface contaminants from an air/liquid interface of a semiconductor processing bath for processing semiconductor wafers.” The method includes “processing said semiconductor wafers in a semiconductor etching solution,” and “rapidly removing an upper portion of said semiconductor etching solution by rapidly removing a wafer boat containing said wafers from said bath, to permit flow of said upper portion of said processing fluid and thereby break surface tension forces holding said surface contaminants at said air/liquid interface.”

Kamikawa et al. discloses a wafer cleaning method in which a wafer cleaning solution is replaced by deionized water before the wafers are removed from the cleaning bath and moved up to a drying chamber. Kamikawa et al. does not disclose or suggest “a method for removing surface contaminants from an air/liquid interface of a semiconductor processing bath for processing semiconductor wafers” which includes “processing said semiconductor wafers in a semiconductor etching solution,” and “rapidly removing an upper portion of said semiconductor etching solution by rapidly removing a wafer boat containing said wafers from said bath, to permit flow of said upper portion of said

processing fluid and thereby break surface tension forces holding said surface contaminants at said air/liquid interface.” Kamikawa et al. does not anticipate or render obvious claim 73.

Claims 10, 27, 62, and 69 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Nishizawa et al. in view of U.S. Pat. No. 5,795,401 to Itoh et al. Applicant traverses this rejection.

Claims 10, 27, 62, and 69 depend from independent claims 1, 17, 61, and 68, respectively. Claim 10 recites that “said upper portion of said etching fluid is removed by a paddle from the top of said wet etching bath.” Claim 27 recites that “said upper portion of said etching fluid is removed from said wet etching vessel by a paddle.” Claim 62 recites that “said upper portion of said semiconductor processing fluid is removed by a paddle from a top of said bath.” Claim 69 recites that “said upper portion of said semiconductor processing fluid is removed by a paddle from a top of said bath.”

Claims 10, 27, 62, and 69 are not rendered obvious by Nishizawa et al., as discussed. Itoh et al. does not cure the deficiencies of Nishizawa et al. Itoh et al. discloses using a “paddle,” (discussed further below) but does not teach or suggest reducing the volume of a treating bath, or removal of any contaminants from the etching bath, much less the removal of “surface contaminants from an air/liquid interface.” Itoh et al. merely refers to the scrubbing of a wafer surface using a rotary brush while pressure is applied by jetting a fluid on the other surface of the wafer. In addition, Itoh et al. does not teach or suggest rapidly removing a substantial portion of the etching liquid. Itoh et al. does not even mention an etching fluid. Itoh et al. refers only to a wash liquid that is purified water and that comes into contact with a rotary brush that cleans the wafer surface. Thus, there is no teaching or suggestion in either of these two references for the claimed subject matter.

Further, Applicant respectfully submits that the proposed combination of references lacks the motivation required for a *prima facie* rejection under 35 U.S.C. § 103. Nowhere does Nishizawa et al. disclose or suggest reducing a volume of the treatment bath. Itoh et al. refers only to the actual physical cleaning and scrubbing of the wafer surface by mechanical means such as a cylindrical rotary brush. The back pressure "paddle" 7 disclosed by Itoh et al. is not analogous to the paddle recited in the claims of the present invention. On the contrary, paddle 7 disclosed by Itoh et al. is a fluid jet device that discharges an inert gas or high purity water as the back pressure fluid. Itoh et al. does not teach or suggest a paddle such as that disclosed and described in the present application which is utilized to reduce the volume of a treatment bath, as shown in Fig. 15, for example. Thus, the proposed combination appears to be based on picking and choosing selected portions of each reference, without regard to the totality of teachings of the references, in an improper attempt to reconstruct the invention using hindsight. Accordingly, a person of ordinary skills in the art could not have been motivated to combine Nishizawa et al. with Itoh et al., and withdrawal of this rejection is respectfully requested. Further, Applicants submit that the proposed combination, even if properly combinable, fails to achieve the claimed invention. For example, the "paddle" disclosed in Itoh et al. will not reduce treatment bath volume as recited in the present claims. Claims 10, 27, 62, and 69 respectfully are submitted as being patentable over the cited Nishizawa et al. and Itoh et al. references.

Claims 63 and 70 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Nishizawa et al. in view of U.S. Pat. No. 5,958,146 to Mohindra et al. Applicant traverses this rejection.

Claim 63 depends on claim 61. Claim 70 depends on claim 68. Claim 63 recites that an "upper portion of said semiconductor processing fluid is removed by

opening a valve in said bath.” Claim 70 recites that an “upper portion of said semiconductor processing fluid is removed by opening a valve in said processing vessel.”

Claims 63 and 70 are not rendered obvious by Nishizawa et al., as discussed above. Mohindra et al. does not cure the deficiencies of Nishizawa et al. Mohindra et al. discloses a cleaning technique for a semiconductor wafer that uses a hot or heated liquid in conjunction with a carrier gas which includes a cleaning enhancement substance. Mohindra discloses the use of control valves in the method of cleaning the semiconductor wafers, and the Office Action points out that “it would have been obvious to one ordinary skill in the art . . . to have provided Nishizawa et al. reference with a valve as taught by Mohindra et al. because the use of valve would have provided another method of removing contaminants from the top of the wafer etching bath.” Although several control valves, and a drain valve 236, are disclosed, Mohindra et al. does not teach or suggest that any of the valves is used for the reducing volume of a treatment bath for rapid removal of “surface contaminants from an air/liquid interface” of an upper portion of the etching fluid, as in the claimed invention. Accordingly, there is nothing in the combination of Nishizawa et al. and Mohindra et al., without the improper use of hindsight reconstruction, to motivate a person of ordinary skills in the art to arrive at the claimed method. Claims 63 and 70 are patentable over Nishizawa et al. and Mohindra et al.

In view of the above, each of the presently pending claims in this application is believed to be in immediate condition for allowance. Accordingly, the Examiner is respectfully requested to pass this application to issue.

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